UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,426	06/19/2001	Daniel Sobek	AMD-E306	4225

7590 05/09/2003

Wagner Murabito & Hao LLP
Two North Market Street
Third Floor
San Jose, CA 95113

EXAMINER
VU, QUANG D

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/885,426	SOBEK ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 02/25/03* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 15-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,477,084 to Eitan in view of US Patent No. 5,879,990 to Dormans et al.

Regarding claim 16, Eitan (figures 7A-F) teaches a process of fabricating a memory cell comprising a substrate that comprises a first region and a second region with a channel therebetween, the method comprising:

forming a gate (112) above the channel of the substrate (166), wherein the gate (112) comprises a polysilicon layer (column 5, lines 66-67);

forming a bitline (104).

Eitan teaches the bitline (104) is the drain (column 6, lines 28-29).

Eitan differs form the claimed invention by not siliciding the bitline. However, Dormans et al. teach siliciding (26) the source/drain (11 and 12) (figures 7-8; column 5, lines 22-28) in a non-volatile memory cell. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Dormans et al. into the method taught by Eitan, since the silicide layers reduce the resistivity of the source/drain.

Regarding claim 15, the combined device teaches forming an oxide [(178) of Eitan (column 9, lines 56-57)] over the silicided bitline.

Regarding claim 17, Eitan differs from the claimed invention by not showing siliciding the polysilicon layer. However, Dormans et al. teach siliciding the polysilicon layer (21) (figures 7-8; column 5, lines 22-28). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Dormans et al. into the method taught by Eitan because the silicide layer reduce the resistivity of the polysilicon gate.

Regarding claim 18, Eitan differs from the claimed invention by not showing the siliciding of the bitline and the polysilicon layer occur simultaneously. However, Dormans et al. teach the siliciding of the source/drain (11 and 12) and the polysilicon layer (21) (figures 7-8; column 5, lines 22-28) occur simultaneously. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Dormans et al. into the method taught by Eitan because the silicide layers reduce the resistivity of the source/drain and the polysilicon gate.

Regarding claim 19, Eitan teaches electron jump into the nitride layer (110) by hot electron injection (column 2, lines 11-17). Eitan also teaches forming a charge-stored region (162) that contains a first amount of charge if the memory device is in the programming state; and forming a layer (160) between the channel and the charge-stored region (162), wherein the layer (162) has a thickness (column 7, line 64 – column 8, line 4). Eitan does not disclose forming a layer between the channel and the charge-trapping region, wherein the layer has a thickness such that the first amount of charge is prevented from directly tunneling into the layer.

It is inherent that the first amount of charge is prevented from directly tunneling into the layer because the first amount of charge (electron) jumps into the charge storage region (the nitride layer [162]) by hot electron injection.

Regarding claim 20, Eitan teaches the charge trapping region (162) comprises nitride (column 7, lines 64-65). It is inherent that the nitride is silicon nitride because it is a conventional charge storage material for non-volatile memory device.

Regarding claim 21, Eitan differs form the claimed invention by not showing the gate comprises an N-type material. However, Dormans et al. teach the gate layer (17) comprises an N-type material (column 4, lines 39-45). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Dormans et al. into method taught by Eitan, since it reduces the resistance of the gate electrode.

Regarding claim 22, Eitan differs from the claimed invention by not showing the gate comprises a polycrystalline silicon. However, Dormans et al. teach the gate comprises a polycrystalline silicon (column 4, lines 39-45). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Dormans et al. into method taught by Eitan, since it is a conventional gate electrode material.

Regarding claim 23, Eitan teaches forming an insulating layer (164) on the charge trapping region (162) (figures 7A-F).

Regarding claim 24, Eitan teaches the insulating layer (164) comprises oxide (column 7, lines 64-65) (figures 7A-F). It is inherent that the oxide is silicon dioxide because it is a conventional gate insulating material for non-volatile memory device.

Regarding claim 25, Eitan teaches the charge trapping region (162) comprises nitride (column 7, lines 64-65). It is inherent that the nitride is silicon nitride because it is a conventional charge storage material for non-volatile memory device.

Regarding claim 26, Eitan teaches the memory cell comprises an EEPROM memory cell (column 1, lines 9-12).

Regarding claim 27, Eitan teaches the memory cell comprises a two-bit memory cell (a left bit [102] and a right bit [104]) (column 6, lines 28-29; column 8, lines 33-34).

Regarding claim 28, Eitan teaches the substrate comprises a P-type substrate (column 8, lines 1-3).

Regarding claim 29, Eitan differs from the claimed invention by not showing the process further comprising scaling the length of the bitline. It would have been ordinary skill in the art at the time the invention was made to scale the length of the bitline, since it has been held that discovering an optimum value of a result effect variable involves only routine skill the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). The length of the bitline also depends on the density of the memory device.

Regarding claim 30, Eitan differs from the claimed invention by not showing the scaling comprises reducing the thermal cycle of the bitline. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the bitline by thermal process, since it is a well known process to reduce or increase the length of the bitline.

Response to Arguments

Applicant's arguments filed 02/25/03 have been fully considered but they are not persuasive.

It is argued, in pages 6-8 of the remarks, that Eitan and Dormans et al. do not teach or suggest a method for fabricating a memory cell comprising forming a gate above the channel of the substrate, wherein the gate comprises a polysilicon layer, prior to forming a bitline. This argument is not convincing because the claim 16 never discloses a method for fabricating a memory cell comprising forming a gate above the channel of the substrate, wherein the gate comprises a polysilicon layer, prior to forming a bitline.

It is argued, in pages 8 and 9 of the remarks, that Eitan and Dormans et al. do not teach the oxide can be grown on the silicide. This argument is not convincing because the oxide can be grown on the silicide (US Patent No. 6,156,644 to Ko et al.; figure 17; column 7, lines 13-18).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv
May 5, 2003

Steven Loke